REMARKS

Claims 1-61 are pending in this application with claims 1, 11, 21, 33, 46, 50 and 54 being independent. Claims 1, 11 and 54 have been amended, and claim 61 has been added.

Applicant acknowledges with appreciation the Examiner's allowance of claims 46-53, and the Examiner's indication that claims 54-57 are directed to allowable subject matter. Claim 54 has been amended in response to the Examiner's objection, and now is believed to be in proper form for allowance.

Claims 11, 14 and 58 have been rejected as being anticipated by Perner (U.S. Patent No. 6,115,019), and claims 19 and 20 have been rejected as being unpatentable in view of Perner. Applicant requests reconsideration and withdrawal of these rejections because Perner does not describe or suggest a liquid crystal display device having n x m storage circuits, n write-in transistors, and n read transistors, where each of the n read transistors controls reading of m storage circuits and each of the n write-in transistors controls writing of m storage circuits, as recited in amended claim 11. According to the Examiner, Perner describes a system that stores at least three frames (i.e., the red, green and blue frames), such that m would equal 3. However, Perner's system includes a write-in transistor 32 and two read transistors 36, 38 for each storage circuit 34, rather than a write-in transistor and a read transistor that control, respectively, writing and reading of 3 storage circuits. Accordingly, for at least this reason, the rejection of claims 11, 14, 19, 20 and 58 should be withdrawn.

Claims 1, 2, 4, 9 and 10 have been rejected as being unpatentable over Okumura (U.S. Patent No. 5,945,972) in view of Perner. Applicant requests reconsideration and withdrawal of this rejection because neither Okumura, Perner, nor any proper combination of the two describes or suggests the arrangement recited in claim 1 of storage circuits, a write-in-storage circuit selector portion, a read storage circuit selector portion, a write-in transistor, and a read transistor. The Examiner asserts that Okumura includes a write-in storage circuit selector portion in the form of an inverter 231, transfer gates 232a and 233a, and switch signal 261, and a read storage circuit selector portion in the form of gates 232b and 233b. Recognizing that Okumara does not

describe or suggest a write-in transistor or a read transistor, the Examiner relies on Perner as describing a write-in transistor 32 electrically connected to a write-in-storage circuit selector portion 14 and read transistors 36, 38 electrically connected to read storage circuit selector portions 18 and 22. The Examiner then asserts that one of ordinary skill in the art would have been motivated to include Perner's transistors 32, 36 and 38 in Okumura's system to allow independent writing and reading operations.

Initially, applicant notes that Perner's control signals 14, 18 and 22 cannot correspond to the recited selector portions because they are not connected to a selected one of the storage circuits, as recited in claim 1. Moreover, applicant strongly disagrees that Perner would have led one or ordinary skill in the art to modify Okumura in order to permit independent writing and reading operations. In particular, since one of Okumura's memories 230a, 230b is written while the other one is read, the write and read operations for a particular memory are already independent of one another, such that Perner would have provided no motivation to modify Okumura.

In addition, using the write operation as an example, both Okumura and Perner describe an arrangement in which a single transistor (e.g., 232a or 32) is used to control write input to a memory (e.g., 230a or 34). As such, absent impermissible hindsight reconstruction of the invention, no combination of Okumura and Perner would have resulted in the recited arrangement in which a write-in storage circuit selector portion is electrically connected to a selected one of the storage circuits and a write-in transistor is electrically connected to the write-in storage circuit selector portion.

For at least the reasons presented above, applicant requests reconsideration and withdrawal of the rejection of claims 1, 2, 4, 9 and 10. In addition, applicant notes that the differences discussed above are further emphasized by new claim 61, which recites that the write-in storage circuit selection portion is electrically connected between the write-in transistor and the selected one of the plurality of storage circuits, and that the read storage circuit selection portion is electrically connected between the selected one of the plurality of storage circuits and the read transistor.

Claim 3 has been rejected as being unpatentable over Okumura in view of Perner and Yamazaki (U.S. Patent No. 5,349,366); claims 5 and 6 have been rejected as being unpatentable over Okumura in view of Perner and Fonash (U.S. Patent No. 5,945,866); claim 7 has been rejected as being unpatentable over Okumura in view of Perner and Johnson (U.S. Patent No. 4,752,118); and claim 8 has been rejected as being unpatentable over Okumura in view of Perner and Kobayashi (U.S. Patent No. 4,432,610). Applicant requests reconsideration and withdrawal of this rejection because neither, Yamazaki, Fonash, Johnson, nor Kobayashi remedies the failure of Okumura and Perner to describe or suggest the subject matter of claim 1.

Claim 12 has been rejected as being unpatentable over Perner in view of Okumura; claim 13 has been rejected as being unpatentable over Perner in view of Yamazaki; claims 15 and 16 have been rejected as being unpatentable over Perner in view of Fonash; claim 17 has been rejected as being unpatentable over Perner in view of Johnson; and claim 18 has been rejected as being unpatentable over Perner in view of Kobayashi. Applicant requests reconsideration and withdrawal of this rejection because neither, Yamazaki, Fonash, Johnson, nor Kobayashi remedies the failure of Perner to describe or suggest the subject matter of claim 11.

With respect to the provisional double patenting rejection of claims 21-45 and 59-60 over claims 3-5 and 8-13 of Application No. 09/912,596, applicant request that this rejection be held in abeyance until the claims of both of these applications are otherwise found to be allowable.

Enclosed is a $1788 check ($18 for excess claim fees, $980 for the Petition for Extension of Time fee, and $790 for the Request for Continued Examination fee). Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 11/1/04

John F. Hayden
Reg. No. 37,640

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

40245126.doc